SPECIFICATION AMENDMENTS:

Please replace the paragraphs starting on page 1, line 8 through page 2, line 4 with the following amended paragraphs:

--With a common process for forming a pattern in fabrication of a semiconductor device, a workpiece film on which a pattern is formed is first formed on the entire surface of a semiconductor substrate, and subsequently, a photo resist film is first formed on the entire surface of the workpiece film. Thereafter, the photo resist film is patterned by the well known photolithographic techniques. A resist pattern formed after being patterned as above is used as a mask in etching of the workpiece film that is an underlying film. Subsequently, the photo resist film is removed, whereupon a pattern of the workpiece film is formed on the semiconductor substrate.

Following a recent increase in the degree of integration in a semiconductor device, miniaturization is required of the minimum line width of the semiconductor device. In order to meet such requirements, it is important to form a superfine resist ~~pattern, however,~~ pattern. However, there has arisen a problem in that requirements for miniaturization beyond a resolution limit cannot be met by use of the conventional photolithographic techniques because there exists a resolution limit due to a wavelength of exposure light used in the formation of a resist pattern.--

Please replace the paragraph bridging pages 2 and 3 with the following amended paragraph:

--However, with the conventional techniques for miniaturization of a resist pattern, a problem has been encountered in that nonuniformity of plasma occurs at the time ashing is applied to the resist pattern, due to a difference in atmosphere inside a plasma chamber, and variation in chemical species. As a result, a pattern shift is susceptible to variation in a wafer surface and among a plurality of wafers, and there has occurred fluctuation in the size of the resist pattern after the ashing. More specifically, with the conventional techniques for miniaturization of a resist pattern, it has been difficult to achieve highly accurate control of size, resulting in occurrence of a problem of deterioration in chip reliability and yield, caused by deterioration in size accuracy.--

Please replace the paragraphs starting on page 5, line 8 through page 7, line 17 with the following amended paragraphs:

--With the process for forming the pattern according to the preferred embodiment of the invention, there is first prepared a silicon (Si) substrate 101 on the surface of which, for example, a semiconductor device, such as a transistor and so forth, is formed. Thereafter, an underlying film 102 that is a workpiece film is formed on the surface of the substrate 101. The underlying film 102 is to be patterned so as to serve as, for example, a gate electrode, wiring, and so forth,

and is made up of a conducting film formed of polysilicon, metal, and so forth. Subsequently, an anti-reflection film 103 is formed to a thickness on the order of 60 nm on the entire surface of the underlying film 102. On top of the anti-reflection film 103, there is applied a positive chemically amplified resist 104 (positive resist UV113 for KrF, manufactured by SIPLEY) to a thickness on the order of about 430 nm, which is to be patterned by irradiation with a first energy beam. As a result of those steps taken as above, there is prepared the substrate 101 with a resist film 104, the anti-reflection film 103, and the underlying film 102, formed on the surface thereof.

Thereafter, a mask 105 with a desired pattern drawn thereon is disposed above the substrate 101 on which the underlying film 102, the anti-reflection film 103, and the resist film 104 are formed in that order, and the substrate 101 is irradiated with a first energy beam, for example, KrF excimer laser beam (λ = 248 nm) 106, thereby transferring the pattern on the mask 105 down to the resist film 104.

With the present embodiment, a half-tone mask with transmittance of light, on the order of about 6%, is disposed above the substrate 101, and a KrF excimer laser beam with an energy amount at about 30 mJ / cm^2 is applied thereto. Further, in the step of irradiation of the present embodiment, use is made of a pattern exposure system with a numerical aperture (NA) at 0.60, using the KrF excimer laser beam for 2 / 3 annular ~~illumination~~ illumination.

After irradiation with the KrF excimer laser beam 106, which is the first energy beam, the resist film ~~104~~ 104, after being ~~exposed~~ exposed, is developed with a solution of about 2.38% tetramethylammonium hydroxide (TMAH), and as shown in Fig. 1(b), a first resist pattern 1041 is formed on top of the anti-reflection film 103. The first resist pattern 1041 formed on top of the anti-reflection film 103 has a width W_1 on the order of about 160 nm. The width W_1 of the first resist pattern 1041 is determined as appropriate depending on pattern-forming conditions and so forth of the pattern exposure system using the KrF excimer laser beam.

With the present embodiment using the positive resist, the resist film in regions irradiated with the first energy beam are rendered easier for ~~removal~~ removal, due to a decomposition reaction with an acid acting as a catalyst, and after a succeeding step of development, the first resist pattern 1041 is formed. More specifically, energy is absorbed by portions of the resist film 104, in the regions irradiated with the first energy beam, thereby generating the acid, and the decomposition reaction is caused to occur to a polymer material contained in the resist film 104 by use of the acid as the catalyst. Thus, the portions of the resist film 104, rendered easier for removal, are removed by use of a developer, thereby obtaining the first resist pattern 1041.

Thereafter, after removal of the mask 105, the first resist pattern 1041 is irradiated with an electron beam that is a second energy beam 107 (EB) (λ =

about 1Å) applied from above the substrate 1 without the use of the mask 105 as shown in Fig. 1(c). At this time, the electron beam, that is, the second energy ~~beam~~ beam, is applied at an energy amount of at least about 2 mC / cm^2, preferably at about 2.8 kcV and on the order of about 4 mC / cm^2. As a result of irradiation of the first resist pattern 1041 with the second energy beam, crosslinking reaction is caused to occur in the first resist pattern 1041.--

Please replace the paragraph bridging pages 8 and 9 with the following amended paragraph:

--The baking process was applied with the baking temperature being varied from 200 to 350°C at intervals of 50°C, and size shrinkage at respective baking temperatures were measured. By plotting the results of the ~~measurement~~ measurements, there was obtained Fig. 2 showing the relationship between the size shrinkage of the resist pattern and the baking temperature at the time of the baking process. Fig. 2 clearly shows that there is an increase in the size shrinkage of the resist pattern wherein crosslinking reaction is caused to occur by applying the second energy beam to the first resist pattern 1041 after formation thereof, in proportion to an increase in the baking temperature, taking place thereafter. The resist pattern formed of the positive resist (UV113) for KrF excimer laser has shrinkage characteristics on the order of about 0.14 nm / °C.--

Please replace the paragraph bridging pages 9 and 10 with the following amended paragraph:

--With the present embodiment, after the crosslinking reaction is caused to occur in the first resist pattern 1041 by applying the second energy beam thereto, heating 108 at 350°C is applied to the first resist pattern 1041 on ~~the public known~~ a conventional hot plate for 60 seconds as shown in Fig. 1(d). As a result, the first resist pattern 1041 with the width W_1 on the order of about 160 nm undergoes shrinkage by about 27.1 nm, thereby forming a second resist pattern 1042 with a miniaturized width W_2 on top of the anti-reflection film 103.--

Please replace the paragraphs starting on page 13, line 18 through page 17, line 19 with the following amended paragraphs:

--As shown in Fig. 3(a), a silicon oxide film ~~202~~ 201 that is an element isolation region is formed on a p-type semiconductor substrate ~~201~~ 202 made up of, for example, a silicon and so forth, by a known LOCOS (local oxidation of silicon) process and so forth.

Thereafter, as shown in Fig. 3(b), a gate insulation film 203, a polycrystalline silicon film 204, an anti-reflection film 205 and a resist film 206 are sequentially formed on the semiconductor substrate ~~201~~ 202. The polycrystalline silicon film 204 is formed by a CVD (chemical vapor deposition) process, then it is processed, and becomes a gate electrode 211 of a transistor. For the resist film 206 formed on the polycrystalline silicon film 204, that is an underlying film, a

material which is the same as the material used in the resist film 104 used in the process for forming the pattern according to the preferred embodiment can be used. According to the method of fabricating the gate electrode of the MOSFET, on top of the anti-reflection film 205, there is applied, for example, a positive chemically amplified resist UV113 for KrF, manufactured by SIPLEY to a thickness on the order of about 430 nm, while rotating, followed by pre-baking treatment at 100°C for 2 minutes, thereby forming the resist film 206.

Then, as shown in Fig. 3(c), a mask 207 with a desired pattern drawn is disposed on the resist film 206, which is irradiated with, KrF excimer laser beam (λ = 248 nm) 208 that is the first energy beam through the mask 207.

Further, in the step of irradiation, the exposure is effected by use of a pattern exposure system with numerical aperture (NA) at 0.60, using KrF excimer laser beam for 2 / 3 annular illumination, and KrF excimer laser beam with an energy amount at about 30 mJ / cm^2 is applied. Further, a half-tone mask with transmittance of light, on the order of about 6%, is disposed above the substrate ~~101~~ 202, and KrF excimer laser beam is applied thereto.

After irradiation with the KrF excimer laser beam 208 that is the first energy beam, the resist film ~~206~~ 206, after being ~~exposed~~ exposed, is developed with a solution of about 2.38% tetramethylammonium hydroxide (TMAH), and as shown in Fig. 3(c), a first resist pattern 2061 is formed on top of the anti-reflection film 205. The first resist pattern 2061 formed on top of the anti-reflection film 205

has a width W_1 on the order of about 150 nm, which is longer by about 20nm compared with the target gate length on the order of 130 nm. The width W_1 of the first resist pattern 2061 is determined depending on conditions of the heat treatment and so forth to be applied later.

Then, after removal of the mask 207, as shown in Fig. 3(d), the first resist pattern 2061 which was is irradiated with the first energy beam is irradiated with an electron beam that is a second energy beam 209 (EB) (λ = about 1Å). At this time, the electron beam is applied at an energy amount of at least about 2 mC / cm^2, preferably at about 2.8 kcV and on the order of about 4 mC / cm^2. As a result of irradiation with the second energy beam, crosslinking reaction is caused to occur in the first resist pattern 2061.

Thereafter, as shown in Fig. 3(e), after the first resist pattern 2061 which was irradiated with the second energy beam is heated 210 by the ~~public known~~ conventional hot plate, to effect a baking treatment. The appropriate conditions of the baking process applied to the first resist pattern 2061 is determined based on the relationship between the heat treatment temperature and the size shrinkage (shrinkage characteristics) of the first resist pattern 2061 which was determined in advance after the irradiation with the second energy beam. With the method of fabricating the MOSFET using the positive resist (UV113), since the width W_1 of the first resist pattern 2061 is on the order of about 150 nm and the target size is on the order of 130 nm, the baking treatment is effected at the temperature of

about 300°C for 60 seconds based on the shrinkage characteristics as shown in Fig. 2 which was determined in advance.

With the baking treatment, the first resist pattern 2061 was miniaturized on the order of about 20nm and the second resist pattern 2062 having the width W_2 on the order of about 130 nm is formed on the anti-reflection film 205.

After the formation of the second resist pattern 2062, as shown in Fig. 3(f), anisotropic etching 212 of the anti-reflection film 205, the polycrystalline silicon film 204 that is the underlying film and the gate insulation film 203 is executed by use of the miniaturized second resist pattern 2062 as a mask, thereby forming the gate electrode 211 having a desired gate length (130nm) on the semiconductor substrate 201.

After the process shown in Fig. 3(f), arsenic (As^+) 214 that is n-type impurity with which the semiconductor substrate 201 is doped by an ion implanter by use of the gate electrode 211 as a mask in the same manner as the ordinary process of fabricating the MOSFET, thereby forming an n-type diffusion layer ~~212~~ on the surface of the semiconductor substrate ~~201~~ 202. Thereafter, a sidewall 213 made up of a silicon oxide film is formed on the semiconductor substrate ~~201~~ 202 including the gate electrode 211 by CVD process and so forth so as to form the structure of an LDD (lightly doped drain) for easing the drain field for restraining the hot carrier effect and so forth. Arsenic (As^+) 214 that is an n-type impurity with which the semiconductor substrate 201 is doped using an ion implanter by use of the gate electrode 211 on which the sidewall 213 is formed as

a mask. As a result, an n^+ type diffusion layer is formed, and a source/drain region 215 having the LDD structure is formed on the surface of the semiconductor substrate ~~201~~ 202. With the foregoing steps, the MOFET having a desired gate length can be achieved.

As described in detail above, according to the method of fabricating the semiconductor device using the process for forming a pattern of the invention, it is possible to fabricate the semiconductor device having a high throughput with highly accurate control of size.

Further, with the method of fabricating the semiconductor device, although the process for forming the pattern when forming the gate electrode that is a part of the MOSFET is exemplified and described, the invention can be applied to the process of forming the other portion, for example, a wiring forming step for electrically connecting to the elements formed on the surface of the semiconductor substrate ~~201~~ 202 and so forth. The underlying film to be patterned at this time forms a conductive film constituting wiring, for example, made up of an aluminium film and so forth.--